

## Single-Mode 100GBASE-SR10 CFP Transceiver



### Особенности:

- Compliant to the IEEE 802.3ba(100GBASE-SR10)
- Compliant to the CFP MSA Specification
- Up to 100m on OM3 and 150m on OM4 MMF
- VCSEL array transmitter and PIN array receiver
- Single 3.3V Power Supply and Power dissipation  $\leq 8W$
- Operates at 10.3125Gbps per channel
- Operating Case Temperature: 0°C~+70°C
- MDIO digital diagnostic interface and control capabilities
- Utilizes a standard 24/20 lane optical fiber with MPO connector

### Области применения:

- 100GBASE-SR10 Ethernet

Part No.	Data Rate	Fiber	Distance *(note2)	Interface	Temp.	DDMI
CFP100G.SR10 *(note1)	100Gbps	MMF	100m/150m	MPO	0°C~+70°C	Yes

Note1: Standard version

Note2: 100m with OM3 MMF and 150m with OM4 MMF

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity(non-condensing)	RH	5	85	%

\*Exceeding any one of these values may destroy the device immediately.

## Recommended Operating Conditions

Parameter	Symbol		Min.	Typical	Max.	Unit
Operating Case Temperature	T <sub>C</sub>	CFP100G.SR10	0	-	+70	°C
Power Supply Voltage	V <sub>CC</sub>		3.2	3.3	3.4	V
Power Dissipation	P <sub>m</sub>		-	-	8	W
Low Power Mode Dissipation	P <sub>low</sub>		-	-	2	w
Aggregate Bit Rate	BR <sub>Aggr</sub>		-	103.125	-	Gbps
Lane Bit Rate	BR <sub>LANE</sub>		-	10.3125	-	Gbps

## Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
<b>Transmitter</b>						
AC common mode input voltage tolerance		-	-	20	mV	RMS
Input Impedance (Differential)	Z <sub>in</sub>	90	100	110	ohms	
Input High Voltage	V <sub>IH</sub>	2	-	V <sub>CC</sub> +0.3	V	3.3V LVCMOS
		0.84	-	1.5	V	1.2V LVCMOS
Input Low Voltage	V <sub>IL</sub>	-0.3	-	0.8	V	3.3V LVCMOS
		-0.3	-	0.36	V	1.2V LVCMOS
<b>Receiver</b>						
Differential output voltage, peak-to-peak		-	-	760	mV	
AC common mode output voltage		-	-	15	mV	RMS
Termination mismatch at 1MHz		-	-	5	%	
Output impedance (Differential)	Z <sub>out</sub>	90	100	110	ohms	
Output rise and fall time		24			ps	20%~80%
Output High Voltage	V <sub>OH</sub>	V <sub>CC</sub> -0.2	-	-	V	3.3V LVCMOS (I <sub>OH</sub> =-100uA)
		1.0	-	1.5	V	1.2V LVCMOS

Output Low Voltage	V <sub>OL</sub>	-	-	0.2	V	3.3V LVCMOS (I <sub>OL</sub> =100uA)
		-0.3	-	0.2	V	1.2V LVCMOS

## Optical and Electrical Characteristics

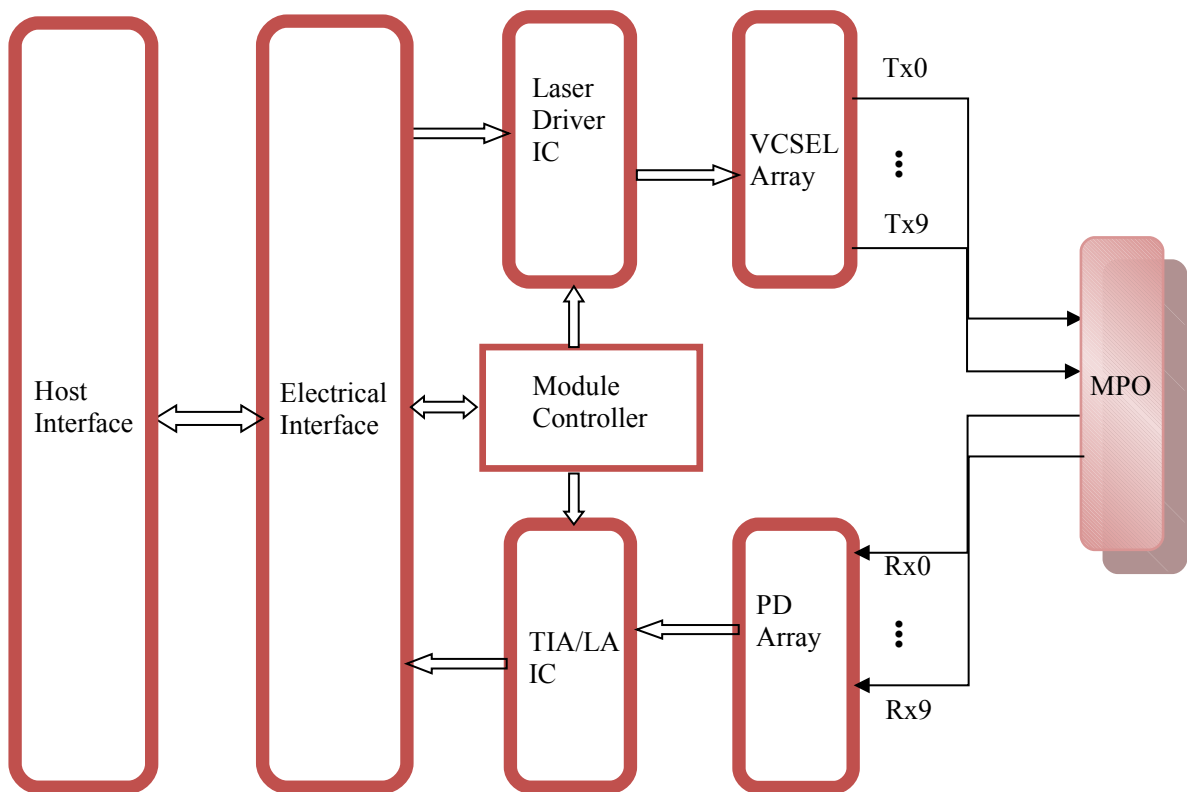
Parameter	Symbol	Min.	Typical	Max	Unit
OM3 MMF	L	0.5	-	100	m
Aggregate Bit Rate	BR <sub>Aggr</sub>	-	103.125	-	Gbps
Per Lane Bit Rate	BR <sub>LANE</sub>	-	10.3125	-	Gbps
<b>Transmitter</b>					
Center Wavelength	$\lambda_c$	840	850	860	nm
RMS spectral width	RMS	-	-	0.65	nm
Average Launch Power, Each Lane <sup>*(note3)</sup>	P <sub>out/lane</sub>	-7.6	-	2.4	dBm
Transmit OMA, per Lane	TX_OMA/lane	-5.6	-	3	dBm
Difference in launch power between any two lanes(OMA)		-	-	4	dB
Peak power, each lane		-	-	4	dBm
Transmitter and dispersion penalty, each lane	TDP/lane	-	-	3.5	dB
Extinction Ratio <sup>*(note4)</sup>	ER	3	-	-	dB
Optical Return Loss Tolerance		-	-	12	dB
Average launch power of OFF transmitter, each lane		-	-	-30	dBm
Output Optical Eye <sup>*(note4)</sup>	IEEE 802.3ba-2010 Compliant				
<b>Receiver</b>					
Center Wavelength	$\lambda_c$	840	850	860	nm
Damage Threshold		3.4	-	-	dBm
Optical modulation amplitude, each lane		-	-	3	dBm
Stressed receiver sensitivity in OMA, each lane		-	-	-5.4	dBm
Average power at receiver input, each lane	RX/lane	-9.5 <sup>*(note5)</sup>	-	+2.4	dBm
Peak power, each lane		-	-	4	dBm
Receiver reflectance	R <sub>r</sub>	-	-	-12	dB

Note3: Output is coupled into a 50/125µm multi-mode fiber.

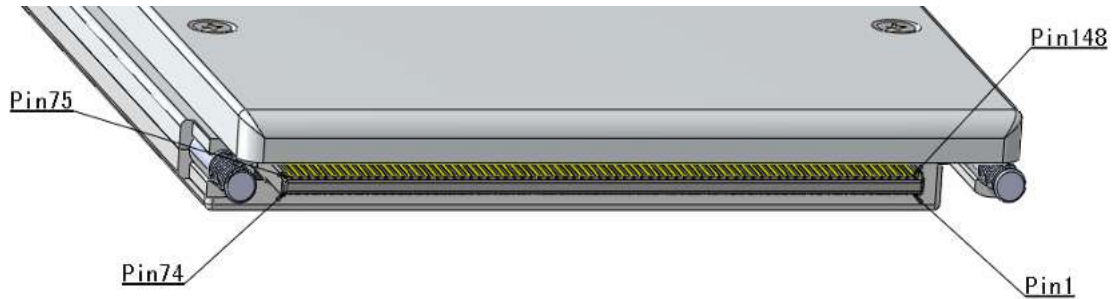
Note4: Filtered, measured with a PRBS  $2^{31}-1$  test pattern @10.3125Gbps

Note5: Minimum average optical power measured at BER less than  $1E-12$ , with a  $2^{31}-1$  PRBS.

### Functional Description of Transceiver



### CFP Transceiver Electrical Pad Layout



	Top Row (2nd Half)		Bottom Row (2nd Half)
148	GND	1	3.3V_GND
147	REFCLKn	2	3.3V_GND
146	REFCLKp	3	3.3V_GND
145	GND	4	3.3V_GND
144	N.C.	5	3.3V_GND
143	N.C.	6	3.3V
142	GND	7	3.3V
141	TX9n	8	3.3V
140	TX9p	9	3.3V
139	GND	10	3.3V
138	TX8n	11	3.3V
137	TX8p	12	3.3V
136	GND	13	3.3V
135	TX7n	14	3.3V
134	TX7p	15	3.3V
133	GND	16	3.3V_GND
132	TX6n	17	3.3V_GND
131	TX6p	18	3.3V_GND
130	GND	19	3.3V_GND
129	TX5n	20	3.3V_GND
128	TX5p	21	VND_IO_A
127	GND	22	VND_IO_B
126	TX4n	23	GND
125	TX4p	24	(TX_MCLKn)
124	GND	25	(TX_MCLKp)
123	TX3n	26	GND
122	TX3p	27	VND_IO_C
121	GND	28	VND_IO_D
120	TX2n	29	VND_IO_E
119	TX2p	30	PRG_CNTL1
118	GND	31	PRG_CNTL2
117	TX1n	32	PRG_CNTL3
116	TX1p	33	PRG_ALRM1
115	GND	34	PRG_ALRM2
114	TX0n	35	PRG_ALRM3
113	TX0p	36	TX_DIS
112	GND	37	MOD_LOPWR

	Top Row (1st Half)		Bottom Row (1st Half)
111	GND	38	MOD_ABS
110	N.C.	39	MOD_RSTn
109	N.C.	40	RX_LOS
108	GND	41	GLB_ALRMn
107	RX9n	42	PRTADR4
106	RX9p	43	PRTADR3
105	GND	44	PRTADR2
104	RX8n	45	PRTADR1
103	RX8p	46	PRTADR0
102	GND	47	MDIO
101	RX7n	48	MDC
100	RX7p	49	GND
99	GND	50	VND_IO_F
98	RX6n	51	VND_IO_G
97	RX6p	52	GND
96	GND	53	VND_IO_H
95	RX5n	54	VND_IO_J
94	RX5p	55	3.3V_GND
93	GND	56	3.3V_GND
92	RX4n	57	3.3V_GND
91	RX4p	58	3.3V_GND
90	GND	59	3.3V_GND
89	RX3n	60	3.3V
88	RX3p	61	3.3V
87	GND	62	3.3V
86	RX2n	63	3.3V
85	RX2p	64	3.3V
84	GND	65	3.3V
83	RX1n	66	3.3V
82	RX1p	67	3.3V
81	GND	68	3.3V
80	RX0n	69	3.3V
79	RX0p	70	3.3V_GND
78	GND	71	3.3V_GND
77	(RX_MCLKn)	72	3.3V_GND
76	(RX_MCLKp)	73	3.3V_GND
75	GND	74	3.3V_GND

### Pin Arrangement and Definition

Pin	Logic	Symbol	Description
1		3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2		3.3V_GND	
3		3.3V_GND	
4		3.3V_GND	
5		3.3V_GND	
6		3.3V	3.3V Module Supply Voltage
7		3.3V	
8		3.3V	
9		3.3V	
10		3.3V	
11		3.3V	
12		3.3V	
13		3.3V	
14		3.3V	
15		3.3V	
16		3.3V_GND	
17		3.3V_GND	
18		3.3V_GND	
19		3.3V_GND	
20		3.3V_GND	
21		VND_IO_A	Module Vendor I/O A. Do Not Connect!
22		VND_IO_B	Module Vendor I/O B. Do Not Connect!
23		GND	
24	CML	(TX_MCLKn)	For optical waveform testing. Not for normal use.
25	CML	(TX_MCLKp)	For optical waveform testing. Not for normal use.
26		GND	
27		VND_IO_C	Module Vendor I/O C. Do Not Connect!
28		VND_IO_D	Module Vendor I/O D. Do Not Connect!
29		VND_IO_E	Module Vendor I/O E. Do Not Connect!
30	LVC MOSw/PUR	PRG_CNTL1	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
31	LVC MOSw/PUR	PRG_CNTL2	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
32	LVC MOSw/PUR	PRG_CNTL3	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤8W, "01": ≤16W, "10":

			≤24W, "1" or NC: ≤32W = not used
33	LVC MOS	PRG_ALARM1	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high power up
34	LVC MOS	PRG_ALARM2	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready
35	LVC MOS	PRG_ALARM3	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
36	LVC MOSw/PUR	TX_DIS	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	LVC MOSw/PUR	MOD_LOPW R	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
38	GND	MOD_ABS	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
39	LVC MOSw/PDR	MOD_RSTn	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
40	LVC MOS	RX_LOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
41	LVC MOS	GLB_ALRMn	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
42	1.2V CMOS	PRTADR4	MDIO Physical Port address bit 4
43	1.2V CMOS	PRTADR3	MDIO Physical Port address bit 3
44	1.2V CMOS	PRTADR2	MDIO Physical Port address bit 2
45	1.2V CMOS	PRTADR1	MDIO Physical Port address bit 1
46	1.2V CMOS	PRTADR0	MDIO Physical Port address bit 0
47	1.2V CMOS	MDIO	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	1.2V CMOS	MDC	Management Data Clock (electrical specs as per 802.3ae and ba)
49		GND	
50		VND_IO_F	Module Vendor I/O F. Do Not Connect!
51		VND_IO_G	Module Vendor I/O G. Do Not Connect!
52		GND	
53		VND_IO_H	Module Vendor I/O H. Do Not Connect!
54		VND_IO_J	Module Vendor I/O J. Do Not Connect!
55		3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56		3.3V_GND	
57		3.3V_GND	

58		3.3V_GND	
59		3.3V_GND	
60		3.3V	3.3V Module Supply Voltage
61		3.3V	
62		3.3V	
63		3.3V	
64		3.3V	
65		3.3V	
66		3.3V	
67		3.3V	
68		3.3V	
69		3.3V	
70		3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
71		3.3V_GND	
72		3.3V_GND	
73		3.3V_GND	
74		3.3V_GND	

## Mechanical Specifications



